CLAIMS

1. An image processing apparatus comprising:

an image storage section adapted to store an image,

an arithmetic section adapted to generate output pixels by arithmetically processing adjacent pixels consisting of M pixels adjoining in the horizontal direction and N pixels adjoining in the vertical direction of the image, the M being an integer of two or more, and the N being an integer of one or more,

a first temporary storage section adapted to readably store the pixels ranging from a Mth pixel to a last pixel in each of horizontal pixel lines of the image,

a second temporary storage section adapted to readably store the pixels ranging from a head pixel to a (M-1)th pixel in each of the horizontal pixel lines of the image, and

a third temporary storage section adapted to delay outputs of the pixels stored in the first temporary storage section, to receive the pixels from the second temporary storage section, and to simultaneously output the adjacent pixels consisting of the M pixels adjoining in the horizontal direction and the N pixels adjoining in the vertical direction to the arithmetic section.

2. An image processing apparatus of claim 1, further comprising a control section,

wherein before the pixels for generating a last output pixel of one of the horizontal pixel lines are stored in the third temporary storage section, the control section reads the pixels ranging from the head pixel to the (M-1)th pixel of the next horizontal pixel line from the image storage section to write them to the second temporary storage section, and

wherein after the pixels for generating the last output pixel of the one of the horizontal pixel lines is outputted from the third temporary storage section to the arithmetic section, the control section reads the pixels ranging from the head pixel to the (M-1)th pixel of the next horizontal pixel line from the second temporary storage section to write them to the third temporary storage section.

3. An image processing apparatus of claim 2,

wherein the N is an integer of two or more, and

wherein with respect to the pixels belonging to the first to the Nth horizontal pixel lines of the image, the control section repeats an operation of sequentially reading the N pixels arranged in the vertical direction from the image storage section and writing the pixels in the first temporary storage section or the second temporary storage section with shifting a reading position in the horizontal direction.

4. An image processing apparatus of claim 3,

wherein the arithmetic section generates the output pixel in every unit time,

wherein the first temporary storage section has N RAMs, and

wherein the control section reads one pixel from the image storage section and writes the pixel to the RAM or the second temporary storage section within the unit time when a previous writing address of the RAM under writing is immediately before a previous reading address, and reads plural pixels from the image storage section and writes the pixels to the RAM and/or the second temporary storage section within the unit when the previous writing address of the RAM under writing is an address two or more immediately before the previous reading address.

5. An image processing method of generating output pixels by arithmetically processing adjacent pixels consisting of M pixels adjoining in a horizontal direction and N pixels adjoining in a vertical direction in an image stored in an image storage section, M being an integer of two or more, and N being an integer of one or more, comprising:

reading the pixels from the image storage section with sifting a reading position in the horizontal direction and writing the pixels in a first temporary storage section;

reading the pixel from the first temporary storage section and writing the pixel in a third temporary storage section;

delaying output of the pixels by the third temporary storage section so as to output the pixels consisting of the M adjacent pixels in the horizontal direction and the N adjacent pixels in the vertical direction to an arithmetic section;

generating the output pixel from the M $\times$ N pixels by the arithmetic section;

before the pixels for generating a last output pixel in one horizontal pixel line is stored in the third temporary storage section, reading pixels ranging from a head pixel to a (M-1)th pixel in the next horizontal pixel line from the image storage section and writing the pixels in a second temporary storage section; and

after the pixels for generating the last output pixel in the one horizontal pixel line are outputted from the third temporary storage section to the arithmetic section, reading the pixels ranging from the head pixel to the (M-1)th pixel in the next line from the second temporary storage section and writing the pixels in the third temporary storage section.

6. An image processing method of claim 5,

wherein the N is an integer of two or more, and

wherein the image processing method further comprising, with respect to the

plural pixels belonging to the first to the Nth horizontal pixel lines of the image, repeating an operation of sequentially reading the N pixels arranged in the vertical direction from the image storage section and writing the pixels in the first temporary storage section or the second temporary storage section with shifting a reading position in the horizontal direction.

7. An image processing method of claim 5,

wherein the arithmetic section generates one output pixel in every unit time,

wherein the first temporary storage section has N RAMs,

wherein one pixel is read from the image storage section and written to the RAM or the second temporary storage section in the unit time when the previous writing address of the RAMs under writing is immediately before the previous reading address, and

wherein the plural pixels are read from the image storage section and written to the RAMs or the second temporary storage section in the unit time when the previous writing address of said RAMs under writing is an address two or more before the previous reading address.